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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/811,031	03/26/2004	Xiaodong Jin	MP0358	1354

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EXAMINER	
BAUER, SCOTT ALLEN	
ART UNIT	**PAPER NUMBER**
2836	

DATE MAILED: 11/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/811,031	JIN ET AL.	
	Examiner	Art Unit	
	Scott Bauer	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 August 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5-11,13-19,21-26,28-32 and 34-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-11,13-19,21-26,28-32 and 34-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-3, 5-7, 9-11, 13-15, 17-19, 21-26, 28-32 &34-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jenkins et al. (US 6,738,248) in view of Duclos (US 5,994,760).

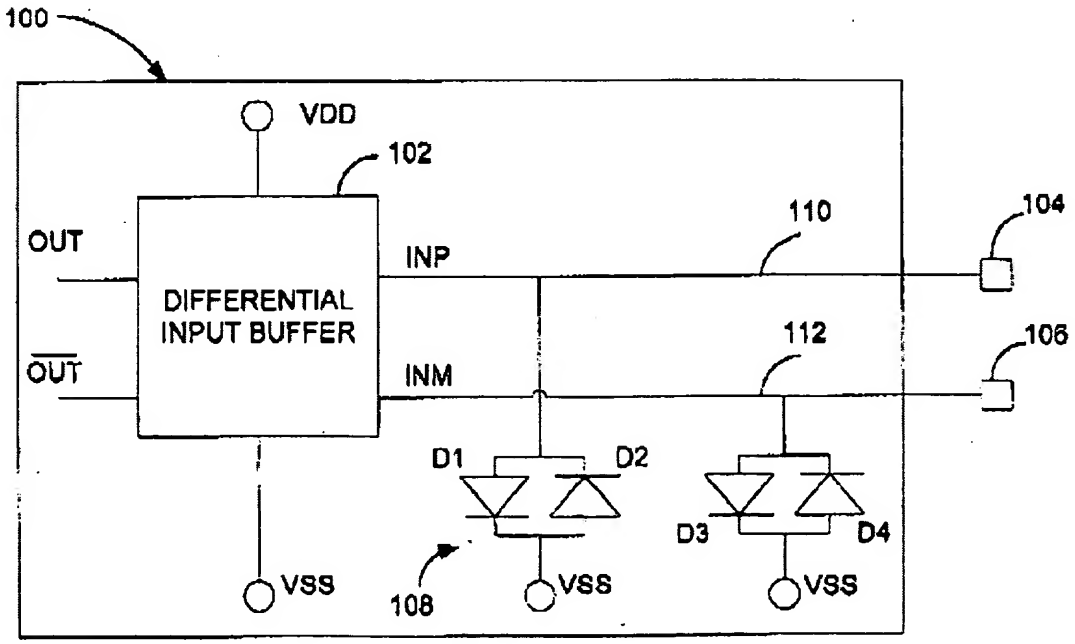

FIG. 1

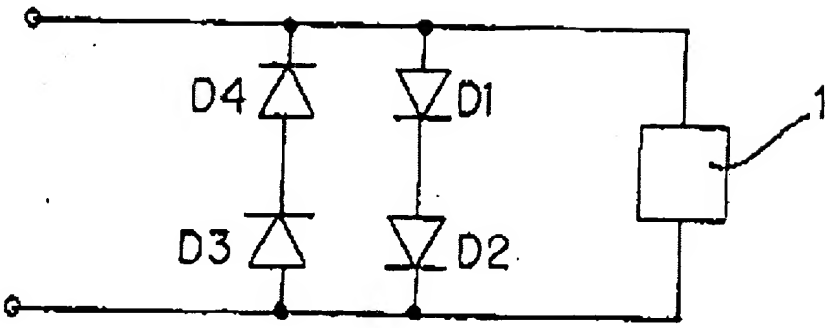

FIG. 2

With regard to Claim 1, Jenkins et al., in Figure 1, discloses a low noise amplifier (100), comprising: a radio frequency input (104); and an electrostatic discharge protection circuit including (108), a pair of diodes (D1 & D2) each having a first and a second terminal; a first diode (D1) of the pair having a first terminal coupled to the radio frequency input (104) and a second terminal directly coupled to a first supply (VSS); a second diode (D2) of the pair having a second terminal coupled to the radio frequency input (104) and a first terminal directly coupled to the first supply (VSS); the electrostatic discharge protection circuit operable to shunt electrostatic discharge current during positive and negative electrostatic discharge events away from the radio frequency input and through the first supply (column 3 lines 34-53).

Jenkins et al. does not teach a separate electrostatic discharge clamp directly coupled between a high voltage supply and a low voltage supply so as to provide a discharge path there between during an electrostatic discharge event.

Duclos, in Figure 2, teaches an electrostatic discharge clamp directly coupled between a high voltage supply and a low voltage supply so as to provide a discharge path there between during an electrostatic discharge event (column 1 lines 49-61).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Jenkins et al. with Duclos, by incorporating the device of Duclos between the terminals VDD and VSS of Jenkins et al., for the purpose of protecting the buffer (102) from ESD occurring from the power supply (column 1 lines 36-39).

With regard to Claim 9, Jenkins et al., in Figure 1, discloses a low noise amplifier (100), comprising: receiving means for receiving an RF input (104); and shunting means (108) including, a pair of diode means (D1 & D2) each having a first terminal and a second terminal; a first diode means (D1) of the pair having a first terminal coupled to the receiving means and a second terminal directly coupled to a first supply; a second diode means (D2) of the pair having a second terminal coupled to the receiving means and a first terminal coupled directly to the first supply; and the shunting means for shunting electrostatic discharge current during positive and negative electrostatic discharge events away from the receiving means and through the first supply (VSS) (column 3 lines 34-53).

Jenkins et al. does not teach a separate electrostatic discharge clamp directly coupled between a high voltage supply and a low voltage supply so as to provide a discharge path there between during an electrostatic discharge event.

Duclos, in Figure 2, teaches an electrostatic discharge clamp directly coupled between a high voltage supply and a low voltage supply so as to provide a discharge path there between during an electrostatic discharge event (column 1 lines 49-61).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Jenkins et al. with Duclos, by incorporating the device of Duclos between the terminals VDD and VSS of Jenkins et al., for the purpose of protecting the buffer (102) from ESD occurring from the power supply (column 1 lines 36-39).

With regard to Claim 17, Jenkins et al., in Figure 3, discloses an electrostatic discharge protection circuit (300), comprising: a pair of diodes (D1 & D2) each having a first terminal and a second terminal; a first diode (D1) of the pair having a first terminal coupled to an input/output pad and a second terminal directly coupled to a first supply; a second diode (D2) of the pair having a second terminal coupled to the input/output pad (104) and a first terminal directly coupled to the first supply; and the electrostatic discharge protection circuit operable to shunt electrostatic discharge current during positive and negative electrostatic discharge events (column 1 lines 36-39).

Jenkins et al. does not teach a separate electrostatic discharge clamp directly coupled between a high voltage supply and a low voltage supply so as to provide a discharge path there between during an electrostatic discharge event.

Duclos, in Figure 2, teaches an electrostatic discharge clamp directly coupled between a high voltage supply and a low voltage supply so as to provide a discharge path there between during an electrostatic discharge event (column 1 lines 49-61).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Jenkins et al. with Duclos, by incorporating the device of Duclos between the terminals VDD and VSS of Jenkins et al., for the purpose of protecting the buffer (102) from ESD occurring from the power supply (column 1 lines 36-39).

With regard to Claim 24, Jenkins et al., in Figure 3, discloses an electrostatic discharge protection circuit (300) for discharging electrostatic discharge events, comprising: shunting means (108) including, a pair of diode means having a first terminal and a second terminal; a first diode means (D1) of the pair having a first terminal directly coupled to an input/output pad (104) a second terminal coupled to a first supply; and a second diode means (D2) of the pair having a second terminal coupled to the input/output pad and a first terminal directly coupled to the first supply; and the shunting means for shunting electrostatic discharge current during positive and negative electrostatic discharge events.

Jenkins et al. does not teach a separate electrostatic discharge clamp directly coupled between a high voltage supply and a low voltage supply so as to provide a discharge path there between during an electrostatic discharge event.

Duclos, in Figure 2, teaches an electrostatic discharge clamp directly coupled between a high voltage supply and a low voltage supply so as to provide a discharge path there between during an electrostatic discharge event (column 1 lines 49-61).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Jenkins et al. with Duclos, by incorporating the device of Duclos between the terminals VDD and VSS of Jenkins et al., for the purpose of protecting the buffer (102) from ESD occurring from the power supply (column 1 lines 36-39).

With regard to Claim 31, Jenkins et al., in Figure 3, discloses a method for discharging electrostatic discharge, comprising: providing a first direct discharge path between an input/output pad and a first supply; providing a second direct discharge path between the input/output pad and the first supply; and shunting electrostatic discharge current during positive and negative electrostatic discharge events through one of the first discharge path and the second discharge path.

Jenkins et al. does not teach providing a third discharge path between the first supply and a second supply during an electrostatic discharge event.

Duclos, in Figure 2, teaches an electrostatic discharge clamp directly coupled between a high voltage supply and a low voltage supply so as to provide a discharge path there between during an electrostatic discharge event (column 1 lines 49-61).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Jenkins et al. with Duclos, by

incorporating the device of Duclos between the terminals VDD and VSS of Jenkins et al., for the purpose of protecting the buffer (102) from ESD occurring from the power supply (column 1 lines 36-39).

With regard to Claims 2,10, 18, & 25, Jenkins et al. in view of Duclos discloses the low noise amplifier of Claims 1, 9, 17, 24 & 31, wherein the first and second diodes are formed by one of polymer devices and metal oxide silicon devices. (column 3, lines 27-33).

With regard to Claims 3, 11, 19, 26 & 32, Jenkins et al. in view of Duclos, in Figure 1, discloses the low noise amplifier of Claims 1, 9, 17, 24 & 31, wherein the first supply is one of a low voltage supply and a high voltage supply, and if the first supply is a low voltage, then the electrostatic discharge protection circuit is not directly coupled to a corresponding high voltage supply, if the first supply is a high voltage supply, then the electrostatic discharge protection circuit is not directly coupled to a corresponding low voltage supply.

With regard to Claims 5, 13, 21, 28 & 34, Jenkins et al. in view of Duclos, in Figure 1, discloses the low noise amplifier of Claims 3, 11, 19, 26 & 32 wherein the positive and negative electrostatic discharge events necessarily include a radio frequency input to high voltage supply positive discharge pulse, a radio frequency input to high voltage supply negative discharge pulse, a radio frequency input to low voltage

supply positive discharge pulse, and a radio frequency input to low voltage supply negative discharge pulse.

With regard to Claims 6, 14, 22, 29 & 35, Jenkins et al., in Figure 3, discloses the low noise amplifier of Claims 5, 13, 21, 28 & 34, wherein the low voltage supply necessarily floats during the radio frequency input to high voltage supply positive discharge pulse and the radio frequency input to high voltage supply negative discharge pulse.

With regard to Claims 7, 15, 23, 30 & 36, Jenkins et al., in Figure 3, discloses the low noise amplifier of Claims 5, 13, 21, 28 & 34, wherein the high voltage supply necessarily floats during the radio frequency input to low voltage supply positive discharge pulse and the radio frequency input to low voltage supply negative discharge pulse.

3. Claims 8 & 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jenkins et al. (US 6,738,248) in view of in view of Duclos (US 5,994,760).

With regard to Claims 8 & 16, Jenkins et al. teaches the low noise amplifier of Claims 1 & 9. Jenkins et al. further teaches that the system is used in a high-speed communication circuit (column 2 lines 37-40).

Jenkins et al. does not teach that the low noise amplifier is compliant with an IEEE standard selected from the group consisting of 802.11, 802.11a, 802.11b, 802.11e, 802.11g, 802.11h, and 802.11i, and 802.14.

However, it would have been obvious to one of ordinary skill in the art at the time the invention was made that a device used in a high speed communication circuit would necessarily be compliant with IEEE standards as the interference created by the device would prevent components that the device relies upon from working properly and to enable the high speed communication circuit to operate and comply with standard industry-wide safety requirements.

Response to Arguments

4. Applicant's arguments with respect to claims 1-3,5-11,13-19,21-26,28-32 and 34-36 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Botker et al. (US 5,764,464) in Figure 5, teaches an ESD protection circuit for a low input bias current circuit wherein a radio frequency input node (V_{INPUT}) is coupled to voltage supply through shunting diodes 522 & 523, which are coupled anti-parallel to each other. A clamping circuit maintains a voltage level between the positive and negative supply. Botker et al. teaches that positive ESD events are shunted to the positive supply through diodes 522 and 520. Negative ESD events are shunted to the negative power supply through diodes 521 and 523 (column 4 lines 20-26).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott Bauer whose telephone number is 571-272-5986. The examiner can normally be reached on M-F 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on 571-272-2058. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SAB
30 OCT 06

Stephen W Jackson
10-30-06

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PRIMARY EXAMINER